**Experiment Report of Digital Logic Circuit with Verilog**

Experiment Information:

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| Index |  |
| Name |  |

Student Information:

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| Student No.： |  |
| Student Name： |  |
| Grade No.: |  |
| Experiment Time： |  |
| Experiment Place： |  |

**Northwestern Polytechnical University**

**School of Computer Science**

**Fall 2019**

*Attention: R****eplace name of this file with your name-student number-report-experiment Index, like XXX-XX-Report-A.docx***

# 1: Object and Requirement

*Tip: introduce the aim of the experiment task. It may cover the function requirement/adopted algorithm/ protocol analyzing/timing requirement/ area requirement*

# 2: Environment and Tools

*Tip: simply introduce the EDA tools you need to complete the experiment.*

# 3: Procedures

*Tip: show the detailed circuit you designed. It may cover:*

*1: the TOP schematic and explanation*

*2: the interface between sub-modules*

*3: the critical timing diagram expected*

*4: the detailed circuit diagram of each submodule*

*5: the verification strategy and the testbench design*

# 4: Result and Discussion

*Tip: what about the result, it may cover:*

*1: whether you have simulated all possible cases*

*2: whether the wave generated by the Modelsim is exactly the same as you expected. You could paste some wave pictures to prove your work.*

*3: whether you have detected some bugs in your code and how to fix them.*

*4: what about the critical path and the area cost.*

*5: how to optimize your design*

*6: whether you have follow some basic coding styles.*

# 5: Conclusion

*Tip:Give a brief conclusion of your work and evaluate your work by yourself.*

# Performance Evaluation

(This part is left only for the instructor)

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| Comment: | Score:  Signature:  Time: |

# Appendix:

(Here, please attach key pieces of code of your design and testbench)